

Fermilab
FY2002 Self-assessment
Process Assessment Report
For
Division/Section: Particle Physics Division

Date: September 25, 2002

Division/Section performing assessment

Particle Physics Division (PPD)

Name of organization that owns assessed process

PPD Electrical Engineering Department, Fixed Target (EED/FT) Projects Group

Organization Strategy

The Electrical Engineering Department, Fixed Target (EED/FT) Projects group has as part of its responsibilities the creation and support of printed circuits for electronics designs primarily done within the Electrical Engineering department. As part of the process of printed circuit board (PCB) production, our ESCAD (Electronics Support Computer Aided Design) group manages the tools, libraries, and archives and does the PCB layouts.

The group also keeps records of PCB vendors and aids in the procurement of prototype boards. This group provides services to others and must keep clear records of when a work request is made and when a job completes. Additionally the group leaders must set priorities and make work assignments based on the complexity of the jobs and the skills of the designers. Traditionally this has been done with a variety of methods from printed logbooks to computerized databases. Since the formation of the ESCAD group a record has been kept that has evolved into a computerized database. This database is being used to prevent jobs from being left hanging incomplete and for monitoring the cycle times. The database is also used to help level the workload among the designers.

The formation of the ESCAD group was predicated on the assumption that designers need specialized skills in order to produce professional quality work. The size of the group was set based upon estimates of workload and it was thought that if we saw the need in the future that the group would be enlarged. By monitoring the job list and completion times we can get a better estimate of whether the size is appropriate for the current workload.

As part of the mission it was thought that defining a uniform set of tools with a quality support team we would be able to improve the delivery times of prototypes and we would be able to reduce the amount of rework. Again to support this concept we believe that appropriate metrics needed to be taken.

Names of Personnel on Assessment team

Marcus Larwill, Tom Wesson

Name of process assessed

Printed Circuit Board Group List of Jobs

Brief description of process to be assessed

The production of a completed PCB requires a number of stages. At the initial stage a work request needs to be logged. The ESCAD leader manages the project assignments and enters the job request into the database. We have three major types of jobs. Parts Library work, PCB layout, and jobs that are mechanical designs. The jobs are entered into the system and after some assessment by the ESCAD leader they are then assigned to a designer. The database is then updated by the designer and monitored by the ESCAD leader. This database is available for read access to the clients of the group.

1. Are metrics associated with this process? If so, what are they?

The metric we will use is new and untested. We currently are assessing the process within the normal management hierarchy and value the subjective information that is being gained. The primary goal being to assess individual work activity and completion times. It was additionally thought that the database would be modified if the need arose. The current PCB tools are also managed under a FLEXLM floating license manager. FLEXLM is a product name for a license manager from Globetrotter software. This tool is capable of recording the use of the tools and providing reports. Additional databases are under design, which will monitor the PCB vendors, but only limited data has been recoded to date.

In addition to the FLEX and ACCESS records there is the actual size of the Parts Library. ACCESS is a database tool that is part of MICROSOFT office. With some careful review of the libraries we can determine the rate of growth of the parts library. There is no way to determine the quality of the parts designs except in the Notes recorded in the ACCESS database. These notes can provide information about what was the status of a board when received from the vendor and if changes in the artwork need to be made. Among the changes are sometime changes that need to be made to the libraries.

With the limited data we could gather we were able to construct a metric composed of the following 5 indicators:

Indicator 1: How well we are recording data into the job list database?

If 80% of all jobs contain the proper information about Requester, Requester Email, Job Name, and Project when entered into the database we will consider our first attempt at using our new tracking system a success (Excellent). A 90% or above proper job entry rate would be considered outstanding.

Indicator 2: Track work assignments. We will note if the jobs entered into the database are also assigned to a designer.

If 80% of the jobs have been assigned then we are Excellent - properly matched for our workload and are not leaving jobs hanging. If we find 90% or better jobs assigned we will consider our assignment of work outstanding.

Indicator 3: Judge if once assigned the jobs are completed within a reasonable time. This is purely an estimate since we have not been tracking our completion rate prior to establishing this database. We would estimate that a job should complete within 6 weeks. That would include the normal Printed Circuit production time since the boards must be returned and any corrections made prior to a job completing. The actual time for the design work would if fact be much shorter.

An average completion time of 6 weeks would be judged as good. An average completion time of 4 weeks or below would be excellent. We would of like to see a 2 week completion rate. That would mean that a design can complete the real design work in one week. We would rate an average completion rate of 2 weeks as outstanding.

Indicator 4: Gage the increase in parts in the library. In this case number of parts the engineers can select from offers a better design environment but quality of parts also matters. This is a slippery indicator but for now total library size will be the indicator.

If we double our library each year we would be doing outstanding work. We would be pleased to see a 25% growth in the library since some parts might be removed and the library cleaned up keeping the size of searches manageable. With modern parts constantly replacing old parts there is no need to maintain a core library for new design that contains parts that should be obsolete.

Indicator 5: Judging the archiving process. We will see which jobs have been archived on the server where there is a regular daily backup.

A 90% job archiving rate would be considered outstanding. Since the designers are working on computers that are networked it is possible for them to archive the data in many ways but we prefer that they place their archives in our central location on the server. This is a new process and will not be considered a requirement of this metric.

What is important for us here is that the job can be located and is backed up on a server that has a regular backup schedule. If at least 60% of the jobs are backed up on the server we will consider our archiving to be good.

To determine our over all performance metric we will score each indicator 1 to 5 points based on the scale:

1. = Unsatisfactory
2. = Marginal
3. = Good
4. = Excellent
5. = Outstanding

These individual indicators will then be totaled and the average taken as the final performance metric.

2. What are the names of the procedures associated with this process?

The JOB REQUEST procedure is the initial stage of each PCB project. Each job that is routed to the ESCAD group should be associated with a Job request form. This form is available on the web along with other related information. The web page provides guidelines on how to prepare a job for the ESCAD group. Clients are expected to provide designs in a format that allows the job to be assumed by the designers and any design advice is best offered prior to the beginning of layout.

The next process is an ASSESSMENT of NEEDS of the job and of the request. Once the job is accepted by the ESCAD group leader, the procedure is to place incoming jobs into a database. The database is known as "List_of_Jobs.mdb". To help manage the archives, the database name has the year added. So the current database is called "List_of_Jobs2002.mdb"

This is a MICROSOFT Access database file.

The next stage would be the DESIGN PROCESS. Jobs are intensively reviewed by designers and subject to frequent communication with the client. This communication process is not monitored but it is clear that some engineers find it harder to hand off jobs to a support group and prefer to be closely involved with the layouts. Completion times are subject to the clients needs and if the job is not properly handed off then the job suffers from frequent rework and adds delays that are not anticipated but that cannot be reduced without the support of personnel outside of the ESCAD group.

The flexIm license manager keeps two types of logs. There is a log that records only the minimal check in and out of the product used by the designers and the client tools such as schematic capture. In addition to this log there is a more extensive report log that records which product sub process was being used. The report log is an encrypted file that requires access to a utility program to view the data. The program used to produce the reports is known as SAMreports. It is from Globetrotter software and due to its cost it is available only on a remote computing division computer.

Also it is the practice of the ESCAD group to keep reasonable work correspondence in

email files. The recommended procedure being to keep a computer record of what changes the client wants so that there is an electronic record that can be accessed for accuracy and to clarify any confusions that might occur in the design process.

It is the DESIGN PROCESS that we spend most of our time with. We also are most interested in minimizing the design time and reducing the number of errors. Most of our monitoring will be concentrated in this process.

The ARCHIVING PROCESS is critical to the integrity of the job. When a jobs reaches a milestone it is placed into the project archives with a date associated with the title of the file. The file is created with a utility built into MICROSOFT office known as WINZIP. This utility is used to compress the file simply to reduce the disk space used. We call the files produced ZIPPED up files of ZIP files. It is recommended that the designer make frequent Zipped up copies of their designs to a work area that is subject to daily nightly back up.

3. Are these procedures being followed? Are they current?

This is the first performance review period and some procedures are still under development. It can be said the basic structure exists to complete the jobs and that there exists adequate communication between the parties involved such that the jobs complete in a timely fashion with a minimum of errors. There are some cases where the procedures are not being followed. Designers have not been reviewed based upon their compliance with the procedures. Engineers have not fully bought into the need for a structured and centralized approach to PCB design.

Also we found cases where projects changed names and become difficult to track. We found designers that put archives in areas other than on our central server. We found that if the procedures were simple and aided the designer and the engineer in the daily work then the procedures were followed. We are attempting to implement easy to use and useful procedures that help minimize errors without adding extra burdens.

The constant updating of tools places a burden of validating the installations and process on the user. This leads to some friction when problems occur and jobs are under time pressures.

For the most part the products we use are up to date and have been tested to be working at a level comparable to past installations. The procedures are current and the web page reflects the changes that have been made. The design procedures we use are a simple reflection of how we have always done it but with the added use of better communication using the internet. The use of floating license for products and the use of servers for support of the tools and procedures provide the clients with a better design environment.

4 Describe the methodology used to assess this process.

This is the first performance review period and some procedures are still under development. We were able to gather some information from the ACCESS database. A visual review of the records combined with the use of EXCEL provided some insight into what has been happening with the jobs that have been logged.

Other more detailed analysis could be made but the information needed is not readily available and would take considerable time to gather with little expected benefit. There are archives of each project. Within the archives are routing completion numbers for each design. This could be recovered with some effort but has not been included in this document.

The primary method used to assess the JOB REQUEST, ASSESSMENT, DESIGN PROCESS, and ARCHIVING process has been concentrate on studying the data in the "List_Of_Jobs.mdb" database. Since this is the first time we have conducted this review it was thought that we should use this opportunity to concentrate on perfecting our jobs database.

5 Results of the assessment:

a. Are the existing process controls adequate?

Prior to this report we were already in the process of implementing changes to our process. There are not plans to improve the process control but the processes for producing and monitoring job status and archival of jobs seems to be in constant evolution.

b. Have any notable practices been identified?

In 100% of the jobs the Requester, RequestorEmail, JobName and Project existed in the database and formed the primary means of identifying the job.
99% of all jobs were listed as having been assigned and the name of a designer was available.

c. Have any major deficiencies been identified?

Still some boards are done in ORCAD. This as a rule is not desired but since some boards existed before we mandated a switch to MENTOR tools, we have a need to continue some designs in the old systems. It might be useful to convert these designs If we cannot simply mandate that all new designs are done in the new system. There also continues to be a lack of knowledge on the part of engineers on how to use the new tool and this combined with schedule pressures is used as an excuse for continuing the use of old tools.

The old tools are not monitored and there is no central control of the libraries or any attempt to share the design information. The use of stand-alone tools like ORCAD should be ended or merged into a centralized design group.

Some engineers fail to provide clear written requirements. There is a frequent problem that engineers are unable to detach the rules of making a PCB design from the actual action of the layout. Some engineers fail to provide clear requirements on the design and see final work as inadequate even if they provided no documents explaining their needs. Frequently the excuse is that it is easier to do it on their own, than to explain to a designer how to do the layout. Some engineers stress that placement of parts is the job of the engineer and not the drafts person.

Some designers failed to update the List_Of_Jobs database. This will be rectified. It is easily monitored and simply by more frequent reminders should be eliminated. It is critical to the evaluation of work that the database has current valid information. When needed new fields can be added. More specific pull down menus can be added to the forms to limit the variations and to help guide the designer in a quick and painless job status entry.

Some designers fail to archive jobs. This must also be eliminated. The drafts people and the engineers must follow proper project management. Jobs must reside in prescribed locations and the data must be placed in locations where daily backup will occur. It is only asking for disaster if the engineer or the drafts person fails to consider the possibility of data corruption or loss due to hardware failure or human error.

Some tools are not working This is already in the process of being rectified. The Flex license tools permit different types of options. One is to keep detailed logs. When multiple tools are installed on a system and multiple licenses are being updated there is sometimes a push to get things running and to neglect the usefulness of statistical data collection. With a little effort on low-pressure days these logs can be re instituted. This has been done for most tools now and we are in the process of testing the log files.

d. Is the process working effectively? What improvements can be made?

The design process is working and the database is established that will permit us to gather information about the availability of our tools and their use. We feel that the system is working well.

Two items remain to be improved. The use of the Web for the dissemination of information has placed pressure on our support staff for keeping the web pages up to date. Additional personnel or more training for current staff might help reduce the problem. For now we place the web page lower on the priority than job completion. We are aware that the current most effective method to distribute information to the department is the web site and email. For this reason constant care will be taken to address our web page needs.

e. How does current performance compare to last assessment, other similar labs, industry?

This is the first reporting period so no comparison can be made this time. No attempt has been made to compare to industry since we feel that our product is unique. There are board houses that we could compare our work to but we do produce a product that requires frequent interaction with the designers and comparisons to industry might not be relevant.

f. What are the results for the metrics?

1. On Our first indicator is the job list database entry we score 5 for OUTSTANDING

The list of jobs for 2002 shows that 98 jobs were entered and of those 66 were

listed as completed. Five of the jobs were listed as in progress while four were listed as started. Five jobs were listed on hold or waiting for data and the remaining 18 jobs failed to have a status entry. Our metric that measures job tracking shows that 97 out of 98 jobs have the proper data to indicate project, job name, requester and requester email.

That is a 99% proper entry rate or a rating of OUTSTANDING (5).

15 jobs were carried over from 2000 and 2001. Of these jobs 5 were listed as not completed. Four of the carried over jobs were listed as "in progress" primarily since they were not limited in scope and have a number of drawings associated with them. This could be considered an important lesson that might be a reflection of some types of work we perform. These four jobs were all mechanical work. Our mechanical files are stored in a separate area.

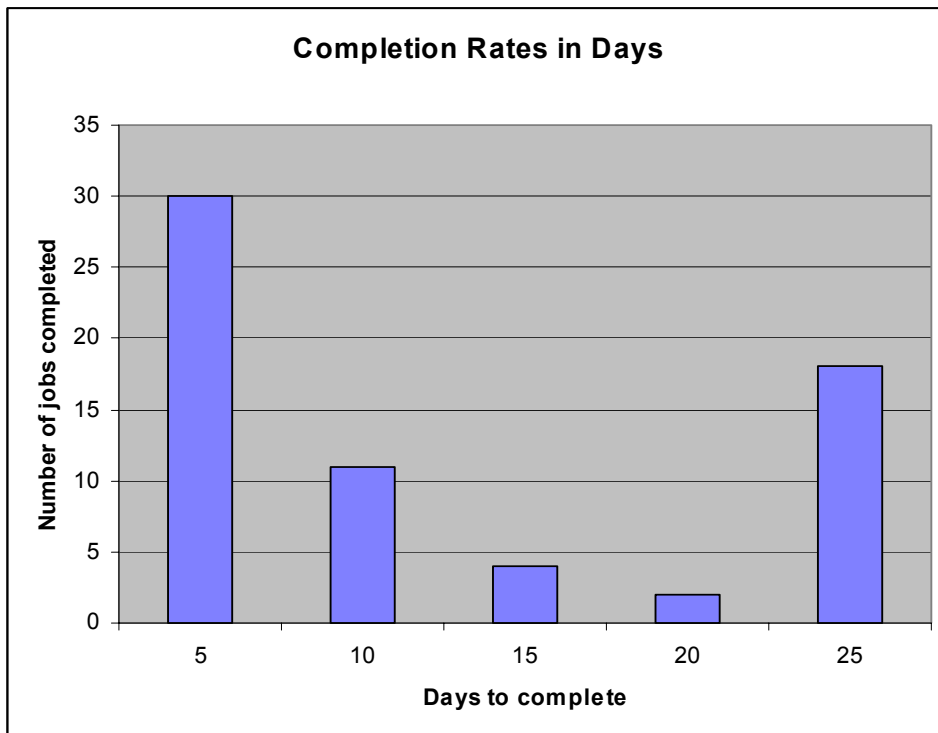
2. On the next indicator the assignment of jobs we scored 5 for OUTSTANDING

Of the 98 jobs all but one was assigned. That job actually was not being handled by the ESCAD group. With 97 out of 98 giving a 99% jobs assigned rate we score an OUTSTANDING (5) rating.

3. Our third indicator was the average time to complete a job scores 4 for EXCELLENT

This appears to be around 3 weeks. This is a remarkable number but it is not a solid measure. It mixes the library updates and a variety of job complexities. The lack of data about board deliveries has made the completion date of a project subject to a great deal of subjective measurement. Our completion time of 3 weeks or around 21 days on average gives us not as good as we wanted but still scores an EXCELLENT rating. By charting and grouping the completion rates into five groups we see that most jobs completed in a week or less. There is also a group of jobs that seem to take longer to complete. These jobs are causing the average to be larger. The graph gives clear indication that there might be at least two types of jobs. We might think this is a group of very hard jobs that take longer but there could be many factors that cause a group of jobs to be slower.

Vacations of the designers or engineers can delay completions. Boards could require rework so mistakes could be the cause of the delays. Boards might be sent out with no need to rush and the board manufacturing could prolong the design cycle. More study is needed to understand the reason for two clusters of jobs.



Our design group is small. Making comparisons of one designer to another based upon data from our database is not fair. The assignments are made based upon skills of the designers and some jobs are much more difficult so they take longer. Attempts to compare the job completion times of different designers, fails to take the job complexity into account.

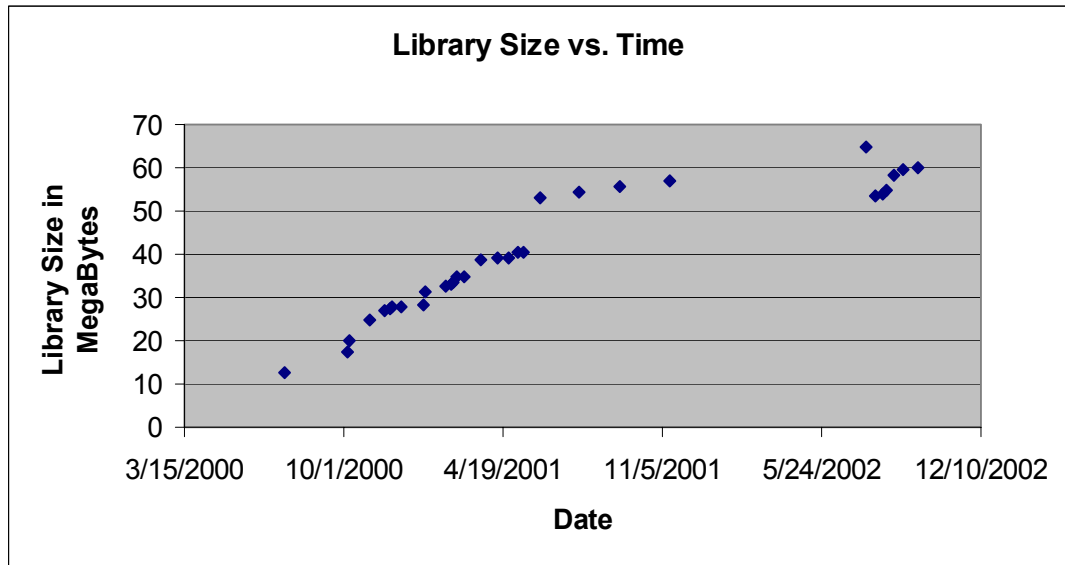
Attempts to compare the quantity of jobs completed also fails to take the complexity of the jobs into account. Two of our designers do most of our layouts. They show the most jobs started but only one of our designers is doing mechanical work and that designer has the least number of jobs. It appears that the mechanical design work has no clear ending. The mechanical design work does not compare directly to the electronic layout work and only subjective measures seem to be possible when comparing productivity and quality.

Indicator 4. Library growth ---- scored 5 for OUTSTANDING

Only one of our designers is doing library management as well as layout. The jobs database does not include any valuable data about the library management. As a result this designer appears to be doing less work but in fact always is working on new parts and has little time for board layout. Again there appears to be missing information in the database and subjective measures are needed to compare designers and to measure workload.

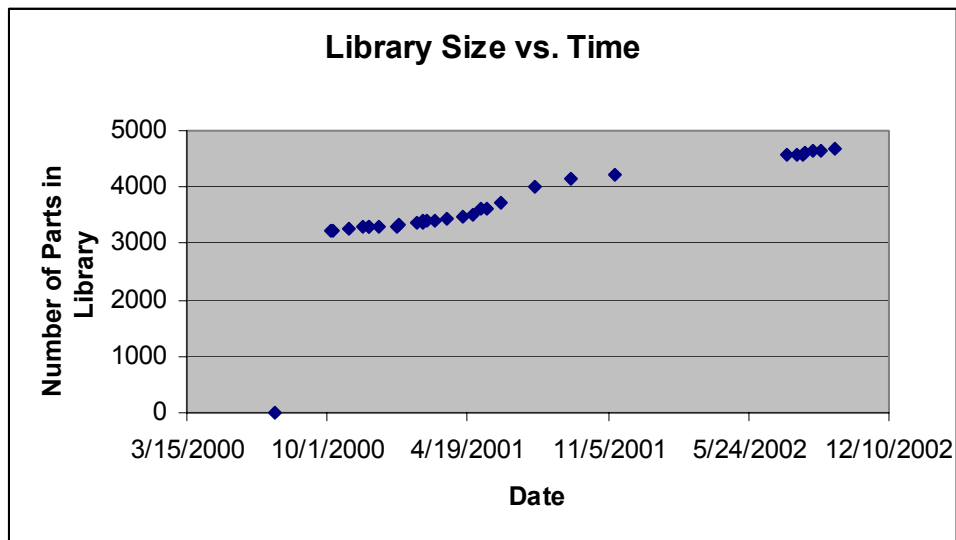
Our fourth indicator is to track the size of the library. A history of the size of the folder containing the library directory was created in EXCEL. A plot was then made

to show the size of the library versus time.



From the chart it can be seen that the size of the actual size of the library grew from 12Megabytes of files space to 60.1Megabytes. This is mainly a reflection of the change in the product. The space used for the library was seriously affected by the upgrade in the software.

When reviewing the total parts in the library we see a large increase due to the addition of a many vendor specific part numbers.



If we use disk space alone as a judge we score a 500% gain in library size. We actually more than doubled our library size two years in a row. This size gain is OUTSTANDING (5). I feel this needs some reassessment for next year.

There is a lack of data in some of the fields. To aid in the database evolution a field was added that is just called NOTES. This field seems to need some work. Some information about jobs could be added in this field but currently fails to be recorded.

Some information could be useful feedback to the designers. Engineers assume that adequate records are being kept by word of mouth but formal processes and records are need to improve the quality of the designs.

5. Archiving rate – scored 3 for Good.

We made an attempt to scan for the archives of all jobs so that we could score our fifth indicator. We have included a spreadsheet that shows of the 98 jobs, 66 were properly archived. This is deceptive since some jobs were in progress and some jobs occurred before we mandated placing them in the archive but we score a 67% archived rate. This is a GOOD rating but not excellent. We hope to do better next year.

Attempts are currently being made to improve the database entry process. Online forms are being constructed that the PCB designers will use to provide information for the database. These forms will have additional fields that will simplify the recording of the job status and quality. The following are two preliminary examples of what we expect will be used soon.

JobName	Assigned
Project	
RqstComp	BRD_Num 0
Started	Num_Lyrs 0
Completed	BRD_Vendor
Status	Gerbers_Sent
Requestor	BRD_Due
RequestorEmail	BRD_Rcvd
Phone_Fax	BRD_Quality

Record: 99 of 99
Form View

Microsoft Access - [Table1]

File Edit View Insert Format Records Tools Window Help

RqstComp	Started	Completed	Assigned	Status	Requestor
Phone_Fax	Project	RequestorEmail	JobName		
BRD_Num	Num_Lyrs	BRD_Vendor	Gerbers_Sent	BRD_Due	BRD_Rcyd
0	0				
BRD_Quality					
Notes					

Record: 99 of 99

When was the Job Finished

g. Adjectival grade achieved

The designers are doing a remarkable job given the constraints. Their work quality is consistently high. Their errors are infrequent and in most cases caught early in the review process. The boards produced usually work due to excellent oversight by the engineers. The boards continue to improve in quality with the experience of the designers. The work being reviewed receives an "A" grade.

The five indicators returned were:

- 1 Proper data entry:--- scored OUTSTANDING =5
- 2 Jobs assigned--- scored OUTSTANDING = 5
- 3 Job completion times --- scored EXCELLENT = 4
- 4 Library growth ---- scored OUTSTANDING = 5
- 5 Archiving rate --- scored GOOD = 3

If we combine the indicators into one metric we pass on all indicators GOOD or above.

By taking the average our total score was 22 with an average of 4.4.

This 4.4 average score means we achieved an overall score of EXCELLENT(4) and just missed the Outstanding category which would begin at a value of 4.5.

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Identified opportunities for improvement

It was initially thought we would be able to include information from the FLEXLM manager. It was found early in the review process that the logging option had not been enabled on the license manager. We were also not able to analyze what limited logs we did have since the SAMREPORTS tool was not readily available on the remote computing division computer. Both these problems are being resolved.

It was also discovered that the designers failed to adequately update the jobs list database. The importance of this has been stress and we are in the process of construction some forms to simplify the updating and reporting process.

It was discovered that extensive information exists within the jobs that is not being recorded. The archives contain much information that can be extracted about the jobs. We are in the process of evaluating how to best extract the information without a great deal of effort.

It was discovered that what one individual considers a completed jobs does not always agree with another designer. Some jobs seem to never end so they never are reported as having ended. This needs further study but it is clear that completion times are not precise. It might be possible to relate completion to the initial delivery of the prototype boards. The analysis of this data might be part of the next review.

Schedule for implementation of improvements

All improvements of our design procedures are currently being implemented. We are constantly are improving our process and have no fixed schedule for any of our changes. We expect that our database will be substantially improved before next year and that the FLEXLM tools will be providing useful information about license usage in the near future.

Status of improvements from previous assessment

No Previous Assessments have been done.

Attachments (supporting data, worksheets, reports, etc.)

The data in the ACCESS database need some analysis that was not available in ACCESS. For this reason we converted the data to an EXCEL format. EXCEL is a spreadsheet product that is part of MICROSOFT office.

Started	Completed	Status	days	complete jobs	Project	JobName
12/31/2000		in progress			CDMS	CDMS Expiriment
12/31/2000		in progress			CDMS	RTF Module
12/31/2000		in progress			infrastr	Infrastructure
6/1/2001		in progress			IB1	IB1 Large Power Supply
1/2/2002	1/15/2002	finished	13	1	Mboone	BPM Signal Select Mod.
2/1/2002		in progress			Auger	Power Control panel
3/1/2002	3/11/2002	finished	10	1	D0_SVX	L0-5_flex_50_cm_21feb02
3/6/2002	3/18/2002	finished	12	1	D0_SVX	DXF2gerber
6/5/2002	6/9/2002	finished	4	1	SDSS	VDC Bulk P.S. Chassis
9/17/2001	12/31/2001	finished	104	1	D0	FPD Transition Patch Pnl
12/20/2001	3/20/2002	finished	90	1	btev	btev pixels
1/2/2002	3/19/2002	finished	77	1	D0	D0 Flex adapter board
1/2/2002	3/28/2002	finished	86	1	D0	D0 Flex adapter_brd_v2
2/4/2002	2/8/2002	finished	4	1	CDF	Claudio Test Board
1/7/2002		hold			D0_SVX	SVX4 finger
1/7/2002	3/10/2002	finished	63	1	D0_SVX	SVX4 Cable
1/7/2002	3/15/2002	finished	68	1	D0_SVX	SVX4 Cable 2
4/1/2002	4/5/2002	finished	4	1	CDF/D0	PLL Daughter board
5/15/2002	5/17/2002	finished	2	1	CDMS	STM parts
5/16/2002	6/19/2002	finished	33	1	EED	FlipChip Bond Brd
6/7/2002	6/11/2002	finished	4	1	SDSS	Autofill cntrl Parts
	6/12/2002	finished	0	1	D0_SVX	SVX4 finger
					Minos	CPLD_Programer
					E881	Parts for Geiger Counter
					CDF	Trigger Inhibit Card Prts
					Beams	Resolver Parts
12/6/2001	1/16/2002	finished	40	1	Mboone	BPM Demodulator 2nd proto
12/1/2001	12/20/2001	finished	19	1	IB1	Config_Volt_Tap
12/17/2001	1/16/2002	finished	29	1	CDF	MP Trigger Panel 2
1/7/2002	1/18/2002	finished	11	1	IB1	Fixed_Tap
1/2/2002	1/18/2002	finished	16	1	IB1	Power Lead
2/11/2002	2/17/2002	finished	6	1	Minos	Menu Test Board
1/23/2002	2/5/2002	finished	12	1	CMS	CCM_Proto1
1/23/2002	1/28/2002	finished	5	1	CMS	CCM_Proto2
1/7/2002	1/23/2002	finished	16	1	CMS	CCM_Proto3
2/10/2002	3/15/2002	finished	35	1	CMS	HF_Backplane
2/7/2002	2/20/2002	finished	13	1	IB1	Coaxial Board
3/18/2002	3/25/2002	finished	7	1	Muon	MFTC_V2

4/22/2002	4/23/2002	finished	1	1	Mboone	PMSS_V2
					CMS	CMS_RADTEST_RS485
					CMS	CMS_RADTEST_AD670
2/19/2002	3/11/2002	finished	22	1	Auger	FEv3_OB
3/4/2002	3/11/2002	finished	7	1	CMS	CCA Test Board V2
3/4/2002	3/11/2002	finished	7	1	CMS	GOL Driver Board V2
3/26/2002	4/5/2002	finished	9	1	CDMS	CDMS_STM_V2
4/2/2002	4/5/2002	finished	3	1	CMS	CCA Test Board V3 (clam)
4/2/2002	4/12/2002	finished	10	1	CMS	CCM_Proto3_Terri
4/16/2002	4/16/2002	finished	0	1	CMS	CCm_Proto2_Standalone
4/11/2002	4/12/2002	finished	1	1	CMS	CCM_Proto3_3U
4/16/2002	4/17/2002	finished	1	1	CMS	LV_Module
5/8/2002					CMS	CCM_Test_Bed
					CMS	SerialBusDriver_V3
					CDF	LVDS2TTL
					E907	Rich2_Card
		started			D0	RMI module Power Supply
					CDMS	CDMS_STM_V2a
					SDSS	SDSS-SC
					CMS	HE_Backplane
					E881	Geiger Counter
		finished	1	1	Auger	dummy_TPCB
					CDF	Repeater_26
					Minos	Burn Test Board
4/23/2002		started			D0	RMI module
2/6/2002	2/18/2002	finished	12	1	D0_SVX	DXF2gerber
5/20/2002	6/5/2002	finished	15	1	D0	VLPC FlipChip Brd
9/17/2001	9/20/2001	finished	3	1	CDMS	Zip RTF Module
11/5/2001	1/11/2002	finished	66	1	Auger	FEv3_Oa1
11/5/2001		started			Auger	FEv3_test
1/23/2002	4/2/2002	finished	69	1	CMS	PMT Base 2X4
	4/2/2002	finished		1	CMS	PMT Base 3X4
2/1/2002	2/14/2002	finished	13	1	Mboone	BPM SS rfswitch
2/1/2002	2/14/2002	finished	13	1	Mboone	BPM SS splitter
2/1/2002	2/14/2002	finished	13	1	Mboone	BPM SS calmod
7/23/2002		waiting			Btev	BtevHVBase
7/23/2002		waiting			Btev	BtevHVSocket
7/16/2002					Btev	BtevHVBoard
2/18/2002	3/19/2002	finished	31	1	CMS	QIE_HPDP_6CH
		waiting			CMS	TTC_Fannout_V2_Board
4/17/2002	5/17/2002	finished	30	1	CMS	PMT_6CH
4/4/2002	5/6/2002	finished	32	1	CMS	CCA Asic TstBrd
6/3/2002	7/17/2002	finished	44	1	CKM	CKM_4Channel_QIE
8/21/2002		finished	0	1	Auger	FEv3_OC
8/6/2002	8/29/2002	finished	23	1	Auger	MicroTPCB_A
8/12/2002	8/29/2002	finished	17	1	Auger	MicroTPCB_B
	8/14/2002	finished	0	1	CDMS	Zip RTF Module V3
4/1/2002	6/5/2002	finished	64	1	CMS	QIE_HPDP_6CHV2
9/21/2001		hold			Fx_Trgt	CMK Base
2/4/2002	2/6/2002	finished	2	1	BTEV	BCH1 (output only)
3/7/2002	3/11/2002	finished	4	1	CDMS	CDMS_STM_V1
3/4/2002	3/6/2002	finished	2	1	D0	SMT_2B
6/10/2002	6/17/2002	finished	7	1	CMS	CCM_Proto3_V2
6/10/2002	6/17/2002	finished	7	1	CMS	CCM_Proto2_V2
6/10/2002	6/17/2002	finished	7	1	CMS	CCM_Proto1_V2
6/10/2002	6/17/2002	finished	7	1	CMS	CCM_Proto1_proasic_V2

6/10/2002		started			D0	L0_Hybrid
6/7/2002	6/19/2002	finished	12	1	CDF	Mini Plug Trans
8/1/2002	8/30/2002	finished	29	1	D0	Mod_Ver_E
					Beams	EPP_Tester
		average		jobs		Resolver
		days=		complete=		
			21.030	66		

The following is the raw data from the ACCESS database know as "List_of_Jobs2002.mdb"

Assigned	Started	Completed	Requestor	Status	JobName	Project
			Client1		Resolve	Beams
Mech Desinger1	12/31/2000		Client2	in progress	infrastructure	infra
Mech Desinger1	12/31/2000		Client4	in progress	CDMS Expiriment	CDMS
Mech Desinger1	12/31/2000		Client3	in progress	RTF Module	CDMS
Mech Desinger1	6/1/2001		Client5	in progress	IB1 Large Power	IB1
Mech Desinger1	1/2/2002		Client6	started	BPM Signal Select	Mboone
Mech Desinger1	2/1/2002		Client7	in progress	Power Control panel	Auger
Mech Desinger1	3/1/2002		Client8	started	L05flex50cm21f	D0SVX
Mech Desinger1	3/6/2002	2/18/2002	Client8	finished	DXF2gerber	D0SVX
Mech Desinger1	6/5/2002	6/9/2002	Client6	finished	VDC Bulk P.S. Chassis	SDSS
Lib Desinger1			Client1		Resolver Parts	Beams
Lib Desinger1			Client9		CPLD_Programer	Minos
Lib Desinger1			Client10		Trigger Inhibit Card	CDF
Lib Desinger1			Client11		Parts for Geiger	E881

Lib Desinger1	6/12/2002		Client12	finished	SVX4 finger	D0SVX
Lib Desinger1	9/17/2001	12/31/2001	Client13	finished	FPD Transition Patch	D0
Lib Desinger1	12/20/2001	3/20/2002	Client14	finished	btev pixels	btev
Lib Desinger1	1/2/2002	3/19/2002	Client15	finished	D0 Flex adapter board	D0
Lib Desinger1	1/2/2002	3/28/2002	Client15	finished	D0 Flex	D0
Lib Desinger1	1/7/2002		Client12	hold	SVX4 finger	D0SVX
Lib Desinger1	1/7/2002	3/10/2002	Client12	finished	SVX4 Cable	D0SVX
Lib Desinger1	1/7/2002	3/15/2002	Client12	finished	SVX4 Cable 2	D0SVX
Lib Desinger1	2/4/2002	2/8/2002	Client16	finished	Claudio Test Board	CDF
Lib Desinger1	4/1/2002	4/5/2002	Client17	finished	PLL Daughter board	CDF/D0
Lib Desinger1	5/15/2002	5/17/2002	Client7	finished	STM parts	CDMS
Lib Desinger1	5/16/2002	6/19/2002	Client18	finished	FlipChip Bond Brd	EED
Lib Desinger1	6/7/2002	6/11/2002	Client19	finished	Autofill cntrl Parts	SDSS
PCB Desinger1			Client20		Rich2_Card	E907
PCB Desinger1			Client19		SDSS-SC	SDSS
PCB Desinger1			Client1		LVDS2TTL	CDF
PCB Desinger1			Client1		Repeater_26	CDF
PCB Desinger1			Client21	finished	dummy_TPCB	Auger
PCB Desinger1			Client9		Burn Test Board	Minos

PCB Desinger1			Client7		CDMS_STM_V2a	CDMS
PCB Desinger1			Client22	started	RMI module Power	D0
PCB Desinger1			Client23		CMS_RADTEST_AD6	CMS
PCB Desinger1			Client23		CMS_RADTEST_RS4	CMS
PCB Desinger1			Client24		HE_Backplane	CMS
PCB Desinger1			Client24		SerialBusDriver_V3	CMS
PCB Desinger1			Client11		Geiger Counter	E881
PCB Desinger1	12/1/2001	12/20/2001	Client25	finished	ConfigVoltTap	IB1
PCB Desinger1	12/6/2001	1/16/2002	Client6	finished	BPM Demodulator 2 nd	Mboone
PCB Desinger1	12/17/2001	1/16/2002	Client26	finished	MP Trigger Panel 2	CDF
PCB Desinger1	1/2/2002	1/18/2002	Client25	finished	Power Lead	IB1
PCB Desinger1	1/7/2002	1/18/2002	Client25	finished	Fixed_Tap	IB1
PCB Desinger1	1/7/2002	1/23/2002	Client23	finished	CCM_Proto3	CMS
PCB Desinger1	1/23/2002	1/28/2002	Client23	finished	CCM_Proto2	CMS
PCB Desinger1	1/23/2002	2/5/2002	Client23	finished	CCM_Proto1	CMS
PCB Desinger1	2/7/2002	2/20/2002	Client25	finished	Coaxial Board	IB1
PCB Desinger1	2/10/2002	3/15/2002	Client24	finished	HF_Backplane	CMS
PCB Desinger1	2/11/2002	2/17/2002	Client9	finished	Menu Test Board	Minos
PCB Desinger1	2/19/2002	3/11/2002	Client21	finished	FEv3_OB	Auger
PCB	3/4/2002	3/11/2002	Client24	finished	GOL Driver Board	CMS

Desinger1					V2	
PCB Desinger1	3/4/2002	3/11/2002	Client24	finished	CCA Test Board V2	CMS
PCB Desinger1	3/18/2002	3/25/2002	Client27	finished	MFTC_V2	Muon
PCB Desinger1	3/26/2002	4/5/2002	Client28	finished	CDMS_STMV2	CDMS
PCB Desinger1	4/2/2002	4/5/2002	Client24	finished	CCA Test Board V3	CMS
PCB Desinger1	4/2/2002	4/12/2002	Client24	finished	CCMProto3Terri	CMS
PCB Desinger1	4/11/2002	4/12/2002	Client24	finished	CCMProto3_3U	CMS
PCB Desinger1	4/16/2002	4/16/2002	Client24	finished	CCmProto2_Standalo	CMS
PCB Desinger1	4/16/2002	4/17/2002	Client24	finished	LV_Module	CMS
PCB Desinger1	4/22/2002	4/23/2002	Client19	finished	PMSS_V2	Mboone
PCB Desinger1	5/8/2002		Client23		CCM_Test_Bed	CMS
PCB Desinger1/cun	4/23/2002		Client22	started	RMI module	D0
PCB Desinger1/we	2/6/2002	2/18/2002	Client8	finished	DXF2gerber	D0SVX
PCB Desinger1/we	5/20/2002		Client29	Started	VLPC FlipChip Brd	D0
PCB Desinger2			Client30	Wait data	TTC_Fannout_V2_Boa	CMS
PCB Desinger2	4/2/2002		Client31	finished	PMT Base 3X4	CMS
PCB Desinger2	8/14/2002		Client7	finished	Zip RTF Module V3	CDMS
PCB Desinger2	2/1/2001	2/14/2002	Client6	finished	BPM SS rfswitch	Mboone
PCB Desinger2	9/17/2001	9/20/2001	Client7	finished	Zip RTF Module	CDMS

PCB Desinger2	11/5/2001	1/11/2002	Client21	finished	FEv3_Oa1	Auger
PCB Desinger2	11/5/2001	2/13/2002	Client21	started	FEv3_test	Auger
PCB Desinger2	1/23/2002	4/2/2002	Client31	finished	PMT Base 2X4	CMS
PCB Desinger2	2/1/2002	2/14/2002	Client6	finished	BPM SS calmod	Mboone
PCB Desinger2	2/1/2002	2/14/2002	Client6	finished	BPM SS splitter	Mboone
PCB Desinger2	2/18/2002	3/19/2002	Client24	finished	QIE_HPD_6CH	CMS
PCB Desinger2	4/1/2002	6/5/2002	Client24	finished	QIE_HPD_6CHV2	CMS
PCB Desinger2	4/4/2002	5/6/2002	Client20	finished	CCA Asic TstBrd	CMS
PCB Desinger2	4/17/2002	5/17/2002	Client24	finished	PMT_6CH	CMS
PCB Desinger2	6/3/2002	7/17/2002	Client21	finished	CKM_4Channel_QI E	CKM
PCB Desinger2	7/16/2002		Client32		btevHVBoard	Btev
PCB Desinger2	7/23/2002		Client32	waiting	btevHVBase	Btev
PCB Desinger2	7/23/2002		Client32	waiting	btevHVSocket	Btev
PCB Desinger2	8/6/2002	8/29/2002	Client21		MicroTPCB_A	Auger
PCB Desinger2	8/12/2002	8/29/2002	Client21	finished	MicroTPCB_B	Auger
PCB Desinger2	8/21/2002		Client21		FEv3_OC	Auger
Manager	9/21/2001		Client32	hold	CMK Base	Fx_Trgt
Manager	2/4/2002	2/6/2002	Client33	finished	BCH1 output only	BTEV
Manager	3/4/2002	3/6/2002	Client34	finished	SMT_2B	D0
Manager	3/7/2002	3/11/2002	Client28	finished	CDMS_STMV1	CDMS
Manager	6/7/2002	6/19/2002	Client10	finished	Mini Plug Trans	CDF

Manager	6/10/2002		Client35	started	L0_Hybrid	D0
Manager	6/10/2002	6/17/2002	Client23	finished	CCM_Proto1prosaic	CMS
Manager	6/10/2002	6/17/2002	Client23	finished	CCM_Proto1V2	CMS
Manager	6/10/2002	6/17/2002	Client23	finished	CCM_Proto2V2	CMS
Manager	6/10/2002	6/17/2002	Client23	finished	CCM_Proto3_V2	CMS
Manager	8/1/2002	8/30/2002	Client29	finished	EPP_Tester	D0

The following is the data used for measuring the archiving:

Started	Completed	Status	Project	JobName	Archive
12/31/2000		in progress	CDMS	CDMS Expiriment	1
12/31/2000		in progress	infrastr	infrastructure	1
12/31/2000		in progress	CDMS	RTF Module	1
2/1/2001	2/14/2002	finished	Mboone	BPM SS rfswitch	1
6/1/2001		in progress	IB1	IB1 Large Power Supply	
9/17/2001	12/31/2001	finished	D0	FPD Transition Patch Pnl	1
9/17/2001	9/20/2001	finished	CDMS	Zip RTF Module	1
9/21/2001		hold	Fx_Trgt	CMK Base	1
11/5/2001	1/11/2002	finished	Auger	FEv3_Oa1	1
11/5/2001	2/13/2002	started	Auger	FEv3_test	
12/1/2001	12/20/2001	finished	IB1	Config_Volt_Tap	
12/6/2001	1/16/2002	finished	Mboone	BPM Demodulator 2nd proto	
12/17/2001	1/16/2002	finished	CDF	MP Trigger Panel 2	
12/20/2001	3/20/2002	finished	btev	btev pixels	1
1/2/2002		started	Mboone	BPM Signal Select Mod.	1
1/2/2002	3/19/2002	finished	D0	D0 Flex adapter board	1
1/2/2002	3/28/2002	finished	D0	D0 Flex adapter_brd_v2	
1/2/2002	1/18/2002	finished	IB1	Power Lead	
1/7/2002	1/23/2002	finished	CMS	CCM_Proto3	1
1/7/2002	1/18/2002	finished	IB1	Fixed_Tap	
1/7/2002	3/10/2002	finished	D0_SVX	SVX4 Cable	
1/7/2002	3/15/2002	finished	D0_SVX	SVX4 Cable 2	
1/7/2002		hold	D0_SVX	SVX4 finger	
1/23/2002	2/5/2002	finished	CMS	CCM_Proto1	1
1/23/2002	1/28/2002	finished	CMS	CCM_Proto2	1
1/23/2002	4/2/2002	finished	CMS	PMT Base 2X4	1
2/1/2002	2/14/2002	finished	Mboone	BPM SS calmod	1
2/1/2002	2/14/2002	finished	Mboone	BPM SS splitter	1
2/1/2002		in progress	Auger	Power Control pannel	1
2/4/2002	2/6/2002	finished	BTEV	BCH1 (output only)	1
2/4/2002	2/8/2002	finished	CDF	Claudio Test Board	1
2/6/2002	2/18/2002	finished	D0_SVX	DXF2gerber	

2/7/2002	2/20/2002	finished	IB1	Coaxial Board	
2/10/2002	3/15/2002	finished	CMS	HF_Backplane	1
2/11/2002	2/17/2002	finished	Minos	Menu Test Board	
2/18/2002	3/19/2002	finished	CMS	QIE_HPDP_6CH	1
2/19/2002	3/11/2002	finished	Auger	FEv3_OB	
3/1/2002		started	D0_SVX	L0-5_flex_50_cm_21feb02	
3/4/2002	3/6/2002	finished	D0	SMT_2B	
3/4/2002	3/11/2002	finished	CMS	CCA Test Board V2	1
3/4/2002	3/11/2002	finished	CMS	GOL Driver Board V2	1
3/6/2002	2/18/2002	finished	D0_SVX	DXF2gerber	
3/7/2002	3/11/2002	finished	CDMS	CDMS_STM_V1	1
3/18/2002	3/25/2002	finished	Muon	MFTC_V2	1
3/26/2002	4/5/2002	finished	CDMS	CDMS_STM_V2	1
4/1/2002	4/5/2002	finished	CDF/D0	PLL Daughter board	
4/1/2002	6/5/2002	finished	CMS	QIE_HPDP_6CHV2	1
4/2/2002	4/5/2002	finished	CMS	CCA Test Board V3 (clam)	1
4/2/2002	4/12/2002	finished	CMS	CCM_Proto3_Terri	
4/4/2002	5/6/2002	finished	CMS	CCA Asic TstBrd	1
4/11/2002	4/12/2002	finished	CMS	CCM_Proto3_3U	1
4/16/2002	4/16/2002	finished	CMS	CCm_Proto2_Standalone	1
4/16/2002	4/17/2002	finished	CMS	LV_Module	1
4/17/2002	5/17/2002	finished	CMS	PMT_6CH	1
4/22/2002	4/23/2002	finished	Mboone	PMSS_V2	
4/23/2002		started	D0	RMI module	1
5/8/2002			CMS	CCM_Test_Bed	1
5/15/2002	5/17/2002	finished	CDMS	STM parts	1
5/16/2002	6/19/2002	finished	EED	FlipChip Bond Brd	
5/20/2002		Started	D0	VLPC FlipChip Brd	
6/3/2002	7/17/2002	finished	CKM	CKM_4Channel_QIE	1
6/5/2002	6/9/2002	finished	SDSS	VDC Bulk P.S. Chassis	1
6/7/2002	6/11/2002	finished	SDSS	Autofill cntrl Parts	
6/7/2002	6/19/2002	finished	CDF	Mini Plug Trans	1
				Mod_Ver_E	
6/10/2002	6/17/2002	finished	CMS	CCM_Proto1_proasic_V2	1
6/10/2002	6/17/2002	finished	CMS	CCM_Proto1_V2	1
6/10/2002	6/17/2002	finished	CMS	CCM_Proto2_V2	1
6/10/2002	6/17/2002	finished	CMS	CCM_Proto3_V2	1
6/10/2002		started	D0	L0_Hybrid	1
7/16/2002			Btev	btevHVBoard	1
7/23/2002		waiting	Btev	btevHVBase	1
7/23/2002		waiting	Btev	btevHVSocket	1
8/1/2002	8/30/2002	finished	D0	EPP_Tester	
8/6/2002	8/29/2002		Auger	MicroTPCB_A	1
8/12/2002	8/29/2002	finished	Auger	MicroTPCB_B	1
8/21/2002			Auger	FEv3_OC	1
			Minos	Burn Test Board	
			CDMS	CDMS_STM_V2a	1
			CMS	CMS_RADTEST_AD670	1
			CMS	CMS_RADTEST_RS485	1
			Minos	CPLD_Programer	
		finished	Auger	dummy_TPCB	
			E881	Geiger Counter	1
			CMS	HE_Backplane	1
			CDF	LVDS2TTL	1
			E881	Parts for Geiger Counter	1
	4/2/2002	finished	CMS	PMT Base 3X4	1

			CDF	Repeater_26	1
			Beams	Resolver	
			Beams	Resolver Parts	
			E907	Rich2_Card	1
	started		D0	RMI module Power Supply	1
			SDSS	SDSS-SC	
			CMS	SerialBusDriver_V3	1
6/12/2002	finished		D0_SVX	SVX4 finger	1
			CDF	Trigger Inhibit Card Prts	
	Wait		CMS	TTC_Fannout_V2_Board	1
	data				
8/14/2002	finished		CDMS	Zip RTF Module V3	1
					66

The following is the data from the EXCEL spreadsheet that we used to calculate our Library size.

Date	File Size	File Name of Compressed Lib	Folder Size (MB)	#of Parts
7/19/2000	2,504,581	Master_Lib_7_19_2000.zip	12.8	0
10/6/2000	2,655,346	TRW_Local_Lib_10_6_00.zip	17.3	3233
10/9/2000	3,146,608	TRW_Local_Lib_10_9_00.zip	20.2	3242
11/2/2000	3,909,387	Fermi_Central_Lib_11200.zip	24.9	3246
11/21/2000	4,403,488	Fermi_Central_Lib112100.zip	26.8	3285
11/28/2000	4,602,967	Fermi_Central_Lib112800.zip	27.4	3292
11/30/2000	4,653,337	Fermi_Central_Lib113000.zip	27.7	3301
12/13/2000	4,676,831	Fermi_Central_Lib_121300.zip	27.8	3306
1/8/2001	4,850,085	Fermi_Central_Lib_1801.zip	28.2	3311
1/12/2001	5,625,799	Fermi_Central_Lib_011201.zip	31.5	3336
2/6/2001	5,853,196	Fermi_Central_Lib_020601.zip	32.4	3371
2/13/2001	6,015,953	Fermi_Central_Lib_021301.zip	33	3381
2/15/2001	6,093,504	Fermi_Central_Lib_021501.zip	33.3	3395
2/20/2001	6,433,447	Fermi_Central_Lib_022001.zip	34.7	3398
3/2/2001	6,519,578	Fermi_Central_Lib_030201.zip	34.9	3419
3/21/2001	7,468,292	Fermi_Central_Lib_32101.zip	38.6	3453
4/13/2001	7,594,475	Fermi_Central_Lib_041301.zip	39.1	3471
4/25/2001	7,645,410	Fermi_Central_Lib_042501.zip	39.2	3523
5/8/2001	7,985,608	Fermi_Central_Lib_050801.zip	40.4	3602
5/15/2001	8,007,990	Fermi_Central_Lib_051501.zip	40.5	3609
6/5/2001	10,045,468	Fermi_Central_Lib_060501.zip	53	3720
7/24/2001	10,345,043	Fermi_Central_Lib_072401.zip	54.3	4020
9/13/2001	10,713,918	Fermi_Central_Lib_091301.zip	55.6	4159
11/15/2001	11,059,800	Fermi_Central_Lib_111501.zip	56.8	4220
7/19/2002	13,063,022	Fermi_Central_Lib_071902.zip	64.9	4563
7/31/2002	10,269,822	Fermi_Central_Lib_7_31_02.zip	53.6	4578
8/9/2002	10,270,478	Fermi_Central_Lib_8_9_02.zip	53.7	4581
8/13/2002	11,212,137	Fermi_Central_Lib_8_13_02.zip	54.7	4604
8/23/2002	11,428,998	Fermi_Central_Lib_8_23_02.zip	58.3	4636
9/3/2002	11,737,539	Fermi_Central_Lib_9_3_02.zip	59.7	4652
9/23/2002	11,819,762	Fermi_Central_Lib_9_23_02.zip	60.1	4672

